Forecasting superconductive electronics technology

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oday's state-of-the-art computer systems are a result of steady, predictable scaling of silicon complementary metaloxide semiconductor (CMOS) integrated circuit technology. In addition, shrinking transistor dimensions over the past several decades have enabled transistor counts as high as seven billion on commercially available processor chips [1]. However, the energy dissipation of CMOS transistors is reaching physical limits and has become a difficult barrier to building more powerful supercomputers [2]. Advances in "beyond-CMOS" device technologies [3–5] are now seen as a key step towards achieving the next major leap in high-performance computing.

At least an order of magnitude improvement in processor energy efficiency will be necessary before exascale supercomputers are viable. The recently announced Chinese Tianhe-2 machine is reported to operate at a record-breaking 33.9 petaflops [6], where one petaflop is a thousand trillion, or 10¹⁵, floating-point operations per second. This performance is achieved by operating close to 80,000 CMOS-based Intel processor chips in parallel. The power consumption of this machine, including the cooling system, is about 24 megawatts. Applying simple scaling, an exascale system providing on the order of 1,000 petaflops would require hundreds of megawatts of power—comparable to a large utilityscale generating station.

One beyond-CMOS technology, digital integrated circuits based on superconductive singleflux-quantum (SFQ) logic, offers a combination of high-speed and ultralow power dissipation unmatched by any other device. First pioneered [7, 8]

at Moscow State University in the 1980s by a team led by Professor Konstantin Likharev [9], SFQ technology has seen a resurgence to address the needs of exascale computing.

Operating at cryogenic temperatures, SFQ devices are based on physical phenomena unique to superconductive circuits. Early SFQ research emphasized ultrahigh-speed operation, highlighted by the experimental demonstration reported in 1999 of an SFQ toggle flip-flop operating at an astounding 770 gigahertz (GHz) [10]. Since then, the emphasis for computing applications has shifted towards energy efficiency. Recent advances in SFQ architectures have allowed researchers to develop small-scale, high-speed computational circuits that dissipate more than one thousand times less power than state-of-the-art silicon CMOS circuits—a large energy advantage even after taking into account power for cryogenic cooling. As a result, superconducting SFQ electronics



technology may prove advantageous for the future of high-performance computing [11].

Superconductive circuit basics

Superconductivity was first observed by Kamerlingh Onnes in 1911 when he experimentally discovered that the electrical resistance of pure mercury dropped dramatically as the sample temperature dropped below 4.2 kelvins (K) [12]. It was not until the 1950s, following basic advances in quantum mechanics and solid-state physics, that a theoretical basis for superconductivity was developed by physicists Bardeen, Cooper, and Schrieffer [13]. Along with the investigation of the Josephson effect in the early 1960s, these experimental and theoretical breakthroughs set the stage for the technology advances in superconductive SFQ electronics.

At the device level, superconductive SFQ electronics technology provides exceptionally fast, low-energy switching—about 1 picosecond (ps) and 10^{-19} joules (J). In addition, and just as important, SFQ electronics technology offers fast and lossless interconnects between circuit elements. A brief look at some highlights of superconductivity physics provides insight into the technology.

First, superconductors can be described as materials that can carry a direct electrical current (dc) in the absence of an electric field. In other words, the materials have zero resistance at dc. A current can flow between two points in a superconductor without a voltage drop or resistive loss. Niobium, one of the most widely used metals for superconductive electronics, has a critical temperature (T)of 9.3 K. Below *T*, niobium is superconductive; above T_c , niobium behaves as a normal metal with electrical resistance.

Superconductors also have very low electrical loss at microwave frequencies. This property enables compact transmission lines for transporting short microwave pulses with minimal energy dissipation at close to the speed of light, in many ways similar to how an optical pulse can be transmitted on optical fiber. This eliminates the capacitive charging energy of interconnects that can dominate the total amount of power dissipation in the most advanced high-speed CMOS circuits.

A second fundamental property of superconductors is flux quantization. The magnetic flux passing through a closed superconducting ring carrying a current is quantized in multiples of the flux quantum expressed simply in terms of fundamental physical constants as $\Phi_0 = h/2e$, about 2 millivolt picoseconds (mV-ps), where h is Planck's constant and *e* is the electron charge. Superconductive SFQ electronics technology is based on the manipulation and transport of these magnetic flux quanta.

Flux quantization results from the quantum mechanical behavior of metallic superconductors. The theory developed by Bardeen, Cooper, and Schrieffer [13] shows that superconducting electrical current results from electron pairing. These electron pairs, now known as Cooper pairs, combine two electrons, one with spin up and one with spin down. With a net spin of zero, Cooper pairs behave as bosons—this means that at very low temperatures they can all fall, or condense, into the ground state, the lowest energy state of the system. The collection of Cooper pairs can thus be described by a single macroscopic quantum mechanical wave function.

The phase variation of the wave function around a closed superconducting ring must be an integer multiple of 2π , and this leads directly to quantization of magnetic flux. This behavior starkly contrasts that of the single unpaired electrons in conventional conductors, which behave as fermions, a type of particle governed by the Pauli exclusion principle. Since no two fermions can occupy the same quantum state simultaneously, condensation of all conduction electrons into a single ground state is not possible.

Realizing active circuits based on manipulating flux quanta requires a means to switch these quanta in and out of superconducting loops. This is accomplished by interrupting the ring with a Josephson junction (JJ), consisting of two superconductors separated by a thin insulating, or barrier, layer. Quantum mechanics predicts that Cooper pairs can tunnel across the barrier layer. As described by the Josephson effect, the junction superconducting current varies periodically with the phase difference ϕ between the wave function on either side of the barrier as $I = I \sin \phi$, where I is the critical current.

In addition, a time-varying change in ϕ results in a voltage drop across the junction.

In the steady state, a JJ can support a constant (dc) superconducting current with zero voltage drop and a phase difference ϕ that remains constant over time as long as the current level does not exceed the junction critical current *I*. If the junction current is forced to exceed *I*_c, then a voltage will develop across the junction along with a time-varying phase ϕ , as indicated in figure 1. Each 2π rotation in ϕ results in the generation of an SFQ voltage pulse of area Φ_o , approximately 2 mV-ps, across the junction. A higher junction voltage corresponds to a faster rate of SFQ pulse generation. The average voltage across a JJ in an SFQ circuit is proportional to the average SFQ switching frequency *f* by the simple relationship $V = \Phi_0 f$. In actual circuits, a

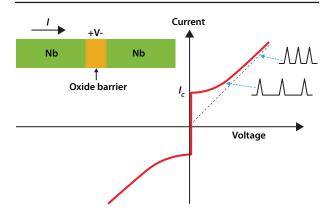


FIGURE 1. This diagram illustrates the current-voltage (I-V) relationship for a niobium (Nb)-based Josephson junction (JJ). A drive current in excess of the critical current I_c results in SFQ pulse generation.

shunt resistor is placed in parallel with the junction to provide damping and well-behaved SFQ pulse generation.

Building circuits and logic gates exploiting SFQ operation involves combining loops and inductors for storing flux along with transformers and JJs for control and switching. A very simple SFQ circuit, shown in figure 2, illustrates the basic mechanism. A superconducting ring is interrupted by a single JJ, and a transformer couples an amount of magnetic flux into the ring proportional to an externally applied control current. If the control current results in the loop current I_i exceeding I_i , then a short voltage pulse will result across the junction along with a 2π phase shift. This corresponds to a single quantum of flux passing through the junction.

The basic SFQ switching operation can be extended to form a complete set of logic functions. A simple example of an SFQ gate is the D-type flip-flop, a key building block of SFQ shift registers and shown as a circuit schematic in figure 3. The D flip-flop has a storage loop formed by the Josephson junctions J₁ and J₂ and the inductor L₂. With a bias current applied to keep J, close to its critical current, an input 'D' (data) pulse entering through J will switch J₁ and inject an SFQ pulse into the storage loop, resulting in an increase in the circulating current *I*_s passing through J₂. Readout is performed with an incoming clock pulse. In the presence of a stored pulse *I*, an incoming clock pulse will cause J₂ to switch, resulting in an output pulse at 'Q'. With no stored pulse, the clock pulse is insufficient to switch J₂ and there will be no output pulse at 'Q'.

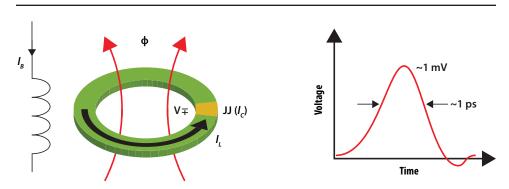


FIGURE 2. This diagram illustrates the generation of an SFQ pulse in a superconducting ring with a Josephson junction (JJ). When the applied current I_o to the transformer results in a circulating loop current I, in excess of the JJ critical current I, an SFQ pulse is generated.

As stated earlier, ultralow energy dissipation is a key attraction of SFQ electronics. The energy dissipated for each basic SFQ switching event is given by the simple expression $\Phi_{o}I_{c}$. For a typical critical current of 50 microamperes (μA), the switching energy is an exceptionally small 1 x 10⁻¹⁹ J.

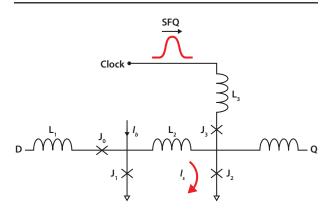


FIGURE 3. This schematic circuit diagram shows an SFQ Dtype flip-flop. The circuit is comprised of Josephson junctions (J_p) forming circuit loops with inductors (L_p) . A bias current I_p is applied to the storage loop. A 'data' input pulse at D results in a stored SFQ pulse which, in the presence of a clock pulse, is transferred to the output Q.

The switching speed varies in proportion to the square root of the JJ critical current density J. For niobium-based technology, a typical J value of 10 kiloamperes per square centimeter (kA/cm²), which provides an I_a of 50 μ A for a junction of area 0.5 μm², results in an SFQ pulse width of only about 1 ps and a maximum gate clock rate of about 350 GHz for small-scale circuits.

Lowering I_c would be a straightforward way to achieve even lower switching energy, but for practical conventional logic circuits where low error rates are required, it is important to operate with switching energies several orders of magnitude higher than the thermal energy $(k_{p}T)$, which at 4 K is about 6 x 10^{-23} J. Just as for CMOS logic circuits which contain multiple switching transistors per logic gate, an SFQ logic operation will require multiple SFQ switching events. With a typical SFQ logic gate configured with roughly five JJs, gate switching is still exceptionally low at about 5 x 10^{-19} J.

To put SFQ switching energy and speed in perspective, comparisons with other advanced high-speed logic technologies are shown in figure 4. The minimum gate-switching energy of the most advanced 10-nanometer CMOS technology is projected to be about 8 x 10⁻¹⁶ J, operating up to about 10 GHz. More than half of this energy is devoted to powering interconnects between transistors. Tunneling field-effect transistors (TFETs) are another beyond-CMOS technology being pursued

for high-speed and low switching energy. Devices based on magnetic spin can operate with very low energy dissipation but only at lower speeds.

The ultralow switching energy of SFQ is only achieved at cryogenic temperatures of about 4 K. From a system perspective, the energy required for refrigeration needs to be taken into account. Modern-day, closed-cycle cryocoolers (e.g., SHI Cryogenics [14]) can readily support projected SFQ processor cooling needs. No ongoing supply of liquid helium is necessary. With efficiencies of roughly 1,000 watts of wall plug power to provide 4 K cooling with 1 watt of heat dissipation, the effective SFQ switching energy is about 10⁻¹⁶ J, which is still nearly an order of magnitude lower than state-of-the-art CMOS.

Superconductive integrated circuit fabrication

Just as with silicon CMOS technology, the ability to fabricate superconductive electronics as planar integrated circuits is crucial to realizing complex and miniature SFQ processors. In fact, many of the

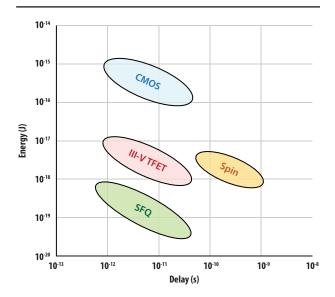


FIGURE 4. The projected gate-switching energy and delay time for several beyond-CMOS technologies (i.e., SFQ, III-V TFET, and Spin) compared with state-of-the-art silicon CMOS illustrates that SFQ switching energy is nearly an order of magnitude lower than state-of-the-art CMOS. [III-V refers to compounds with elements from both columns III and V of the periodic table.]

basic fabrication steps and processing tools for SFQ are borrowed directly from standard silicon integrated circuit technology.

Today, the most widely used JJ technology for very-large-scale integrated SFQ circuits is based on trilayers of niobium/aluminum/aluminum oxide/niobium. In a typical fabrication sequence, the niobium base electrode, aluminum layer, and niobium counter electrode are deposited by sputtering. The ultrathin (about 1 nanometer) aluminum oxide insulating tunnel barrier is formed by partial oxidation of the aluminum layer during this trilayer deposition process. The junction critical current density *J*₂ is set primarily by the thickness of the tunnel barrier. Individual JJ circuit elements are patterned by photolithography and reactive ion etching. Accurate targeting of junction critical current *I* is realized by precise and reproducible control of photolithography and etch processes, along with high accuracy and uniformity of the starting trilayer J_{\cdot} .

Multilayer SFQ fabrication processes are required to build complex circuits with dense interconnections between cells or gates. A 10-layer niobium process, with the cross-section shown in figure 5, is under development at Massachusetts Institute of Technology (MIT) Lincoln Laboratory. Circuits are fabricated on eight-inch silicon wafers with a single JJ layer. Superconductive niobium wiring layers are patterned for inductors. Metal wiring layers are separated by dielectric, and vias are used to interconnect layers to form circuits. A separate resistive layer is deposited and patterned for shunt resistors. All layers can be patterned by photolithography and etching. Chemical-mechanical planarization is employed at various steps in the process to maintain yield and uniformity. The lower metal layers can be used for interconnections between cells with passive transmission lines. A photomicrograph of a small portion of a fabricated SFO chip fabricated at MIT Lincoln Laboratory in an eight-layer process is shown in figure 6.

Several foundry processes have been developed worldwide and circuits with tens of thousands of JJs have been successfully demonstrated. In the US, Hypres, Inc. [15, 16] offers a four-layer standard process, with an option for six niobium layers,

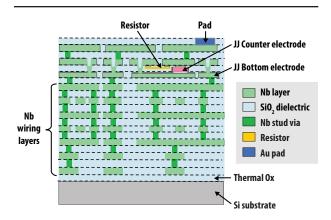


FIGURE 5. This diagram shows a cross section of a 10-layer niobium (Nb) SFQ microfabrication process under development at MIT Lincoln Laboratory. The circuits are fabricated on silicon (Si) substrates with a thermal oxide (Ox) layer. The Nb wiring layers are separated by silicon dioxide (SiO₂) dielectric layers. Gold (Au) pads are used for wirebond attachment to external circuits.

patterned with deep-ultraviolet photolithography to realize smaller feature sizes. The Superconductivity Research Laboratory of the International Superconductivity Technology Center (ISTEC) in Japan has developed a 10-layer niobium process (ADP2) for large-scale SFQ circuit demonstrations [17]. In Europe, the FLUXONICS Foundry for superconductive circuits has developed a three-layer niobium process [18]. A major emphasis of their work is on SFQ interface electronics for high-performance superconductor sensor applications.

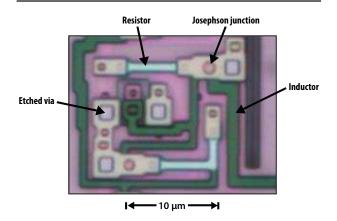


FIGURE 6. This photomicrograph shows an SFQ integrated circuit (at partial completion for visibility) with key circuit elements indicated.

Building blocks for SFQ processors

To date, the unique properties of SFQ electronics have already been exploited to demonstrate complex circuits for diverse applications. For radar and communications, a large effort in the US developed SFQ analog-to-digital converters based fundamentally on the speed and precision of flux quantization [19]. High-precision superconductor analog-to-digital converters comprised of approximately 5,000 JJs have been demonstrated at sampling rates of tens of gigasamples per second [20]. This work has been extended to successfully demonstrate [21] complete SFQ-based multichannel receivers including both digitizers and digital-signal processors on chips comprising about 11,000 JJs. Other efforts, particularly in Europe, have focused on SFQ implementations of readout circuits for cryogenic detectors [22]. Finally, SFQ circuits are being investigated as candidates for readout and control of superconductive qubits for quantum computing.

For high-performance computing applications, work has focused on developing computation building blocks such as adders and multipliers, which in turn can be configured into arithmetic logic units for general-purpose processors. Early efforts, initiated over a decade ago, included technology demonstrations of complete, but simple, microprocessors including the FLUX [23] and CORE [24] chips, with approximately 65,000 and 11,000 JJs, respectively. Efforts now are emphasizing scalable high-performance designs and architectures.

Significant work is under way on SFQ arithmetic circuits. A 16-bit sparse-tree adder, for example, was recently demonstrated by researchers from Stony Brook University, Yokohama National University, and Nagoya University [25]. The adder, designed to operate with rapid single-flux quantum (RSFQ) logic at 30 GHz with latency, the time required to calculate the output sum, of only 352 ps, is comprised of 9,941 JJs occupying an area of 8.5 square millimeters (mm²). The same team has also demonstrated a low-latency eight-bit multiplier in the ISTEC 10 kA/cm² 1.0 µm fabrication process [26]. The RSFQ multiplier operates at 20 GHz with a latency of only 447 ps and is comprised of 5,948 JJs in an area of 3.5 mm².

Path to ultralow power

Over the past several years, new SFQ design approaches have been demonstrated which promise to bring circuit power consumption down close to theoretical limits. These advances in SFQ technology are key to addressing the energy efficiency needs of high-performance computing.

While SFQ circuits have fundamentally low dynamic switching energy or power, the high static or standby power associated with providing dc bias currents in earlier SFQ circuits would typically dominate the power budget. A typical SFQ gate, such as the D-flip-flop described above, requires a bias current I, through each junction during gate operation where I_{ι} is typically comparable to I_{\cdot} . Until recently, most SFQ circuit designs, including the SFQ logic family RSFQ, employed a resistive bias network to provide a stable dc bias current to each junction [8]. This resulted in a static bias power of about 800 nanowatts (nW) per gate which, for a gate operating as fast as 20 GHz, is about 60 times higher than the dynamic power dissipation [27]. For demonstrating the high-speed capability of SFQ circuits of modest complexity, this static power dissipation was not a major concern; however, minimizing energy usage is essential for large-scale SFQ computing applications.

New SFQ design families reduce the static power consumption to near zero. These techniques all involve removing or minimizing resistive circuit elements in the bias network. Some low-power design approaches, such as energy-efficient rapid single-flux quantum (ERSFQ), aim to reduce power with changes in bias circuitry only, while otherwise using existing RSFQ gate designs. Other recently developed approaches for ultralow power, such as reciprocal quantum logic (RQL), are based on entirely new logic designs.

In ERSFQ [28], and a similar approach called eSFQ [29], dc bias currents are delivered to SFQ gates via a superconductive bias network where resistors are replaced by current-limiting JJs feeding each gate. As the JJ current-voltage (*I-V*) curve in figure 1 indicates, with a very small dc applied voltage, the dc current will remain very close to the critical current I_c . Clocking schemes devised for ERSFQ and eSFQ ensure that the correct current-limiting operation of the bias JJs is maintained during dynamic gate-switching operation. In addition, bias line inductors are employed in these schemes to minimize bias current fluctuations during circuit operation. The size of these inductors, particularly for ERSFQ, can be relatively large, thus impacting overall logic density.

Another ultralow power SFQ design approach is RQL [30]. Here, dc bias lines are replaced by multiphase alternating-current (ac) power lines. All gates are inductively coupled to the ac power line and therefore no static power is dissipated on chip. The multiphase ac bias also serves as the clock for RQL circuits, replacing SFQ-base clock distribution networks.

An ultralow power RQL adder has been demonstrated by Northrop Grumman [31]. The eight-bit design employs a Kogge-Stone carry-look-ahead architecture and is implemented on a 5 mm x 5 mm chip with 815 junctions. The circuit was fabricated in the Hypres foundry process. Operating at a clock rate of 6.2 GHz, the power dissipation was only 510 nW. The authors project that a 64-bit adder would have a latency of only two clock cycles at 20 GHz in a more advanced fabrication process.

Path to higher integration

To meet future supercomputer needs, any beyond-CMOS technology must be scalable to high levels of integration. Reported exascale hardware designs envision SFQ processors with 20 million JJs [11]. This calls for circuit densities of at least one million JJs per square centimeter, nearly 10 times higher than integration levels typically reported today. High SFQ circuit density can be achieved through combining advances in several different aspects of SFQ technology as indicated in the development progression shown in figure 7.

As a first step, providing a sufficient number of metal wiring layers to enable efficient circuit layouts is essential for achieving high density. The 10-layer process shown in figure 5, for example, allows vertical stacking of circuit interconnections under logic cells, resulting in significant savings in chip area.

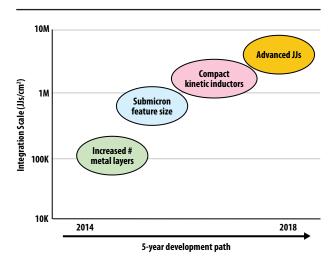


FIGURE 7. This diagram shows the development path for highly integrated SFQ processors.

With this approach, compact vias are also important for layer interconnections.

Reducing feature size is also an important step; however, the scaling rules for SFQ integrated circuits are very different than those for CMOS-based transistor circuits. Looking back at the photomicrograph in figure 6, the relative sizing of the circuit elements of a typical SFQ cell are readily apparent. The JJs, which are approximately 1 μ m in diameter, are much smaller than the inductor and shunt resistor. While increasing junction J_c 's and shrinking junction diameter could increase speed and therefore computational throughput, only a modest improvement in circuit density would result. This is because inductance values vary inversely with I_c , and I_c is generally constrained by noise and energy considerations.

Fortunately, reducing feature size is a way to shrink inductors. A typical SFQ cell inductor with a 1 μ m-wide metal trace would require inductor lengths as long as approximately 10 μ m. By reducing feature sizes down to 0.5 μ m, the same inductance values could be reached in less than half the area.

Another way to shrink inductors is to take advantage of the so-called kinetic inductance of superconductors. This is a result of the physical momentum related to ballistic transport of charge in superconductors, which has no counterpart in normal conductors. Compact kinetic inductors fabricated from the superconductor niobium nitride look particularly attractive [32].

Finally, there are two promising research directions in advanced JJs which could provide a further boost to circuit density. The first is on self-shunted junctions which would eliminate the need for external shunt resistors. Forming JJs using amorphous niobium-silicon barrier layers is one approach being pursued [33]. Another research direction exploits the properties of JJs with a ferromagnetic tunnel barrier [34, 35]. This special type of device, called a π -junction, has a built-in π phase shift of the superconductive wave function. This reduces the phase shift necessary to generate across the inductor during gate switching, thus reducing the necessary inductance value. These ferromagnetic junctions are also being pursued as an SFQ-compatible memory element.

Conclusion

The past several years have seen major strides in the development of advanced superconductive SFQ digital electronics to meet the needs of future energy-efficient, high-performance computer systems. Fast SFQ computational circuits have been demonstrated operating on 100 times less power than comparable silicon CMOS circuits. New fabrication processes and circuit designs promise increased circuit complexity and integration.

About the author

The Massachusetts Institute of Technology Lincoln Laboratory is a federally funded research and development center that applies advanced technology to problems of national security. Research and development activities focus on long-term technology development as well as rapid system prototyping and demonstration. These efforts are aligned within its key mission areas: space control; air and missile defense technology; communication systems; cybersecurity and information sciences; intelligence, surveillance, and reconnaissance systems and technology; advanced technology; tactical systems; homeland protection; air traffic control; and engineering. The laboratory works with industry to transition new concepts and technology for system development and deployment.

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